correspond to at least one of data storage devices **311-313**. The general operation of a demultiplexer is understood in the art; as such, those of skill in the art will appreciate that demultiplexer **350** may include additional signal input lines. In some embodiments, demultiplexer **350** may include a plurality of routing devices arranged in logical rows to form a logical binary tree. Demultiplexer **350** may include additional signal input lines (not shown) such that each logical row of routing devices is controlled by a respective signal input line.

The above description of illustrated embodiments is not intended to be exhaustive or to limit the embodiments to the precise forms disclosed. Although specific embodiments of and examples are described herein for illustrative purposes, various equivalent modifications can be made without departing from the spirit and scope of the disclosure, as will be recognized by those skilled in the relevant art. The teachings provided herein of the various embodiments can be applied to other quantum computing systems, methods and apparatus, not necessarily the exemplary quantum computing systems, methods and apparatus generally described above.

For instance, the foregoing detailed description has set forth various embodiments of the systems, methods and apparatus via the use of block diagrams, schematics, and examples. Insofar as such block diagrams, schematics, and examples contain one or more functions and/or operations, it will be understood by those skilled in the art that each function and/or operation within such block diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof.

The various embodiments described above can be combined to provide further embodiments.

All of the U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification including, but not limited to: U.S. Pat. No. 6,838,694; US Patent Publication No. 2005-0082519; US Patent Publication No. 2006-0225165; U.S. Provisional Patent Application Ser. No. 60/872,414, filed Jan. 12, 2007, entitled "System, Devices and Methods for Interconnected Processor Topology"; U.S. Provisional Patent Application Ser. No. 60/956,104, filed Aug. 16, 2007, entitled "Systems, Devices, And Methods For Interconnected Processor Topology"; U.S. Provisional Patent Application Ser. No. 60/986,554, filed Nov. 8, 2007, entitled "Systems, Devices and Methods for Analog Processing"; US Patent Publication No. 2006-0225165; US Patent Publication No. 2006-0147154; U.S. Provisional Patent Application Ser. No. 60/913,980, filed Apr. 25, 2007, and entitled "Adiabatic Superconducting Qubit Logic Devices And Methods"; U.S. Provisional Patent Application Ser. No. 60/917,884, filed May 14, 2007, entitled "Scalable Superconducting Flux Digital-To-Analog Conversion Using A Superconducting Inductor Ladder Circuit"; U.S. Provisional Patent Application Ser. No. 60/917,891, filed May 14, 2007, entitled "Systems, Methods, And Apparatus For A Scalable Superconducting Flux Digital-To-Analog Converter"; and U.S. Provisional Patent Application Ser. No. 60/975,487, filed Sep. 26, 2007, entitled "Systems, Methods and Apparatus for a Differential Superconducting Flux Digital-to-Analog Converter" are incorporated herein by reference, in their entirety and for all purposes. Aspects of the embodiments can be modified, if necessary, to employ systems, circuits and concepts of the various patents, applications and publications to provide yet further embodiments.

These and other changes can be made to the embodiments in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the invention to the specific embodiments disclosed in the specification and the claims, but should be construed to include all possible embodiments along with the full scope of equivalents to which such claims are entitled. Accordingly, the scope of the invention shall only be construed and defined by the scope of the appended claims.

What is claimed is:

1. A quantum processor comprising:

a plurality of programmable devices including a plurality of qubits; and

a memory administration system including a plurality of communication conduits, wherein the memory administration system is configured to couple to at least one of the programmable devices via at least one of the communication conduits, and wherein the memory administration system includes at least one digital-to-analog converter (DAC).

2. The quantum processor of claim **1** wherein at least one programmable device and at least a portion of the memory administration system are formed by a material that is superconducting below a critical temperature.

3. The quantum processor of claim **1** wherein the programmable devices are selected from the group consisting of superconducting flux qubits, superconducting charge qubits, superconducting phase qubits, superconducting hybrid qubits, quantum dots, trapped ions, trapped neutral atoms, qubit couplers, superconducting qubit couplers, impurities, nuclear spin qubits, electronic spin qubits, and photonic qubits.

4. The quantum processor of claim **1** wherein at least one communication conduit is configured to communicably couple between two or more programmable devices.

5. The quantum processor of claim **1** wherein the memory administration system comprises a plurality of components and at least one communication conduit is configured to communicably couple between at least one programmable device and at least one component of the memory administration system.

6. The quantum processor of claim **1** wherein the memory administration system comprises a plurality of components and at least one communication conduit is configured to communicably couple between two or more components of the memory administration system.

7. The quantum processor of claim **1** wherein the DAC includes a superconducting flux DAC, and wherein digital signals are represented by discrete magnetic flux quanta.

8. The quantum processor of claim **1** wherein the memory administration system includes at least one memory register.

9. The quantum processor of claim **8** wherein at least two memory registers are configured to communicably couple in series with one another.

10. The quantum processor of claim **8** wherein at least one memory register is configured to administer digital signals to at least one DAC.

11. The quantum processor of claim **10** wherein at least one memory register is configured to administer digital signals to at least one DAC in the form of magnetic flux quanta.

12. The quantum processor of claim **10** wherein at least one memory register is configured to galvanically couple to at least one DAC.

13. The quantum processor of claim **10** wherein at least one memory register is configured to inductively couple to at least one DAC.

14. The quantum processor of claim **8** wherein the memory administration system includes a superconducting flux-based shift register.